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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,990	03/24/2004	Samson Huang	42P15059D	6775

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EXAMINER	
XIAO, KE	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
10/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,990	HUANG ET AL.	
	Examiner	Art Unit	
	Ke Xiao	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 6,288,764) in view of the Applicant's Admitted Prior Art (AAPA).

Regarding **Claim 1**, Zhang teaches an integrated circuit, comprising:

a first glass substrate (Zhang, Fig. 1 base glass substrate);

a light modulation structure formed on a first are of the substrate (Zhang, Fig. 1 active matrix circuit portion with liquid crystal cells); and

a cover glass covering the light modulation structure and secured to the substrate on a second area of the substrate, wherein at least a portion of an active circuit is formed on the second area of the substrate (Zhang, Fig. 1 element 108 and 100 driving circuitry).

Zhang fails to teach a silicon substrate. The AAPA teaches that silicon substrates are well known in the art for use in liquid crystal displays (AAPA, Pg. 1 paragraph [0006]). It would have been obvious to one of ordinary skill in the art to replace the

glass substrate of Zhang with the silicon substrate as taught by the AAPA in order to increase performance of the driver circuitry (AAPA, Pg. 1 paragraph [0006]).

Regarding **Claim 2**, Zhang further teaches that the light modulation structure comprises a pixel array (Zhang, Fig. 1 element 200).

Regarding **Claims 3-5**, Zhang further teaches that the cover glass is secured to the substrate by an adhesive on the second area, and wherein all of the of the active circuit is located under the adhesive (Zhang, Fig. 1 element 104).

Regarding **Claim 6**, Zhang further teaches that the adhesive comprises an adhesive strip defining an enclosed perimeter (Zhang, Figs. 1 and 11).

Regarding **Claim 7**, Zhang further teaches that the adhesive strip comprises an epoxy bead (Zhang, Col. 3 lines 30-35).

Regarding **Claim 8**, Zhang further teaches that the active circuit comprises a memory circuit (Zhang, Col. 7 lines 50-55).

Claims 9-14 and 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 6,288,764) in view of the Applicant's Admitted Prior Art (AAPA), Ikeda (US 2003/0076282) and Negishi (US 5,907,314).

Regarding **Claim 9**, Zhang in view of the AAPA fail to teach a first frame buffer and second frame buffer.

Ikeda teaches a single frame memory can be added to the substrate of a single display system (Ikeda, Figs. 1-3). It would have been obvious to one of ordinary skill in

the art at the time of the invention to add a frame buffer on the substrate of Zhang in view of the AAPA in order to lower power consumption (Ikeda, Figs. 3 and 4, Pg. 1 paragraphs [0015-0016]).

Zhang in view of the AAPA and Ikeda fail to teach a second frame buffer. Negishi teaches two independent display systems can be put on a single substrate (Negishi, Figs. 10 and 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to duplicated the display system of Zhang in view of the AAPA and Ikeda on a single substrate as taught by Negishi in order to provide independent control to a top half and a bottom half of the display.

Regarding **Claim 10**, Zhang teaches a single chip liquid crystal on glass imaging device (Zhang, Fig. 1 and 11), comprising:

an on-chop light modulator on the chip (Zhang, Fig. 1 element 200 and 105).

Zhang fails to teach a liquid crystal on silicon imaging device. The AAPA teaches that silicon substrates are well known in the art for use in liquid crystal displays (AAPA, Pg. 1 paragraph [0006]). It would have been obvious to one of ordinary skill in the art to replace the glass substrate of Zhang with the silicon substrate as taught by the AAPA in order to increase performance of the driver circuitry (AAPA, Pg. 1 paragraph [0006]).

Ikeda teaches a single frame memory can be added to the substrate of a single display system (Ikeda, Figs. 1-3). It would have been obvious to one of ordinary skill in the art at the time of the invention to add a frame buffer on the substrate of Zhang in

view of the AAPA in order to lower power consumption (Ikeda, Figs. 3 and 4, Pg. 1 paragraphs [0015-0016]).

Zhang in view of the AAPA and Ikeda fail to teach a second frame buffer. Negishi teaches two independent display systems can be put on a single substrate (Negishi, Figs. 10 and 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to duplicated the display system of Zhang in view of the AAPA and Ikeda on a single substrate as taught by Negishi in order to provide independent control to a top half and a bottom half of the display.

Regarding **Claim 11**, Zhang further teaches that the light modulator comprises a pixel array (Zhang, Fig. 1 and 11).

Regarding **Claim 12**, Zhang in view of the AAPA, Ikeda and Negishi further teaches a cover glass covering the light modulator and secured to the chip by an adhesive, wherein at least a portion of the on-chip dual frame buffers is formed on the chip under the adhesive (Zhang, Fig. 1, the adhesive portions covers all peripheral driving circuits including the frame buffers).

Regarding **Claims 13 and 14**, Zhang in view of the AAPA, Ikeda and Negishi further teaches that all of the on-chip dual frame buffers is located under the adhesive (Zhang, Fig. 1, the adhesive portions covers all peripheral driving circuits).

Regarding **Claim 20**, Zhang teaches a display system, comprising:

a light engine (Zhang, Fig. 11f element 2502);

a projection lens (Zhang, Fig. 11f element 2504); and

a single chip liquid crystal on glass imaging device configured to receive light from the light engine, encode the light from the light engine with image information, and provide the encoded light to the projection lens (Zhang, Fig. 11f element 2503).

Zhang fails to teach a silicon substrate. The AAPA teaches that silicon substrates are well known in the art for use in liquid crystal displays (AAPA, Pg. 1 paragraph [0006]). It would have been obvious to one of ordinary skill in the art to replace the glass substrate of Zhang with the silicon substrate as taught by the AAPA in order to increase performance of the driver circuitry (AAPA, Pg. 1 paragraph [0006]).

Zhang in view of AAPA fail to teach an on-chip frame buffer. Ikeda teaches a single frame memory can be added to the substrate of a single display system (Ikeda, Figs. 1-3). It would have been obvious to one of ordinary skill in the art at the time of the invention to add a frame buffer on the substrate of Zhang in view of the AAPA in order to lower power consumption (Ikeda, Pg. 1 paragraphs [0015-0016]).

Zhang in view of the AAPA and Ikeda fail to teach a second frame buffer. Negishi teaches two independent display systems can be put on a single substrate (Negishi, Figs. 10 and 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to duplicated the display system of Zhang in view of the AAPA and Ikeda on a single substrate as taught by Negishi in order to provide independent control to a top half and a bottom half of the display.

Regarding **Claim 21**, Zhang further teaches a pixel array (Zhang, Fig. 11).

Regarding **Claims 22-24**, Zhang in view of the AAPA, Ikeda and Negishi further teaches a cover glass covering the pixel array and secured to the single chip imaging device by an adhesive, wherein all of the on-chip dual frame buffers is formed on the chip under the adhesive (Zhang, Fig. 1 element 108 and 104 which cover all of the drive circuitry).

Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US 2003/0076282) in view of the AAPA.

Regarding **Claim 15**, Ikeda teaches a liquid crystal on glass imaging device (Ikeda, Figs. 1-3), comprising:

a cover glass (Ikeda, Fig. 17 elment 3056);

a glass backplane physically connected to the cover glass in a connection area (Ikeda, Fig. 17 base glass substrate and 3065); and

a liquid crystal sealed between the cover glass and the silicon backplane (Ikeda, Fig. 17 element 3063);

wherein the glass backplane comprises:

a frame buffer configured to store pixel data (Ikeda, Fig. 3 element 201);

a pixel array (Ikeda, Fig. 3 element 207);

an interface control block connected between the frame buffer and the pixel array, the interface control block being adapted to determine amplitude

modulation waveforms for the pixel array in accordance with the pixel data stored in the frame buffer (Ikeda, Fig. 3 element 205);

an external interface block configured to provide an external interface to the device, including receiving pixel data and transferring the received pixel data into the frame buffer (Ikeda, Pg. 15 paragraph [0239]); and

a control block connected to the external interface block, the frame buffer, and the interface control block, the control circuit being adapted to provide control signals to operate the device (Ikeda, a control block as claimed is inherent to the system of Ikeda in order to synchronize all of the display driving components).

Ikeda fails to teach a liquid crystal on silicon imaging device with a silicon backplane. The AAPA teaches that silicon substrates are well known in the art for use in liquid crystal displays (AAPA, Pg. 1 paragraph [0006]). It would have been obvious to one of ordinary skill in the art to replace the glass substrate of Ikeda with the silicon substrate as taught by the AAPA in order to increase performance of the driver circuitry (AAPA, Pg. 1 paragraph [0006]).

Regarding **Claim 16**, Ikeda further teaches that the frame buffer block includes memory cells collocated with pixel elements of the pixel array (Ikeda, Fig. 3 located on the same substrate).

Regarding **Claim 17**, Ikeda further teaches that the frame buffer includes a front buffer and a back buffer (Ikeda, Fig. 5 top and bottom halves of the buffer).

Regarding **Claim 18**, Ikeda further teaches that the frame buffer, the interface control block and the control block are located on a periphery of the device and at least partially fit within the connection area where the cover glass is attached to the backplane (The connection area is the area between the substrates, and since the frame buffer is formed on the base substrate is also located within the connection area as claimed).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US 2003/0076282) in view of the AAPA as applied to Claims 15-18 above, and further in view of Negishi (US 5,907,314).

Ikeda in view of the AAPA fail to teach that the frame buffer, the interface control block and the pixel array are divided into first and second parts as claimed. Negishi teaches two independent display systems can be put on a single substrate (Negishi, Figs. 10 and 11). It would have been obvious to one of ordinary skill in the art at the time of the invention to duplicated the display system of Ikeda in view of the AAPA and Ikeda on a single substrate as taught by Negishi in order to provide independent control to a top half and a bottom half of the display.

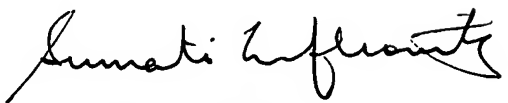
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ke Xiao whose telephone number is (571) 272-7776. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 11th, 2007 - kx -



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